ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

DET - Design, Simulation, and Fabrication of Planar MOS Quantum Dot for Spin-Based Quantum Computing

Funded By	Dipartimento DET
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Context of the research activity	This PhD project addresses the technology-oriented development of quantum dot devices for spin qubits. It combines automated simulation of quantum confinement and transport in planar MOS structures with fabrication-aware modeling, enabling realistic assessment of device performance, scalability, and manufacturability using established processes suitable for research-scale production-
	Quantum computing is widely recognized as a transformative technology capable of addressing computational problems that are beyond the capabilities of classical computers. Among the various physical implementations under investigation, semiconductor spin qubits hosted in silicon quantum dots represent one of the most promising routes toward scalable quantum processors, due to their long coherence times and intrinsic compatibility with MOS manufacturing technologies. This PhD project aims to develop and apply a fully automated, fabrication-aware simulation framework for the design, optimization, and technological assessment of semiconductor quantum dot devices intended as host platforms for spin qubits. The core objective is to establish a robust link between quantum device physics and realistic semiconductor fabrication processes, enabling the evaluation of device concepts that are not only theoretically viable but also manufacturable using established MOS technologies. The research focuses primarily on planar MOS architectures fabricated on silicon-on-insulator (SOI) substrates. This platform was selected due to its high technological maturity, extensive documentation in the literature, and proven compatibility with industrial MOS process flows. Importantly, planar SOI MOS structures remain feasible for implementation in low-volume research laboratories (as Piquet facilities at Politecnico di Torino), providing

Objectives	an optimal balance between experimental accessibility and long-term scalability. Quantum confinement and charge transport simulations are carried out using QTCAD, a state-of-the-art solid-state quantum simulation platform developed by Nanoacademic Technologies Inc. Device geometries are created using parametric three-dimensional models in Fusion (Autodesk), allowing rapid and systematic exploration of design parameters. Parametric geometry definitions enable efficient design iterations, ensuring that modifications to physical dimensions or layout can be seamlessly propagated throughout the simulation workflow. A key innovative aspect of this project is the integration of quantum device simulations with realistic fabrication process modeling. Once the quantum behavior of a given device geometry is validated, the architecture is transferred to Synopsys Sentaurus Process to simulate MOS-compatible fabrication steps, including material deposition, etching, oxidation, and dopant diffusion. The results of these process simulations are then used to refine the original device design, which is subsequently re-simulated at the quantum level. This iterative, closed-loop methodology enables the systematic optimization of both device performance and process feasibility. The developed framework is applied to a set of representative device architectures, including planar single and double quantum dots, as well as selected three-dimensional structures such as FinFET-like and nanowire gate-all-around devices. These architectures are chosen to explore the impact of geometry and electrostatic control on qubit confinement, transport behavior, and technological robustness. All devices are evaluated with respect to their suitability as scalable spin qubit platforms. The project also concerns the interaction with the microelectronics integrated front-end necessary for contro, writing-reading of Qubits state. The expected outcome of this project is a versatile and extensible simulation framework capable of supporting fabrication-oriented design decisions for quantum dot spin qubit devices. By incorporating realistic process modeling and enabling systematic studies of design and technology trade-offs, the project directly contributes to the development of scalable, MOS-compatible quantum hardware. Future extensions will include the assessment of process variability and non-idealities, providing critical insights into device robustness, yield, and manufacturability—key requirements for the transition from laboratory-scale demonstrations to large-scale quantum computing systems.

Skills and competencies for the development of the activity	Solid background in semiconductor device physics, with particular emphasis on MOS structures and nanoscale devices Fundamentals of quantum mechanics and solid-state physics, including quantum confinement and electron transport Knowledge of fabrication processes, such as photolithography, oxidation, deposition, etching Experience with or strong interest in TCAD tools (e.g. Sentaurus Process, Sentaurus Device, or equivalent) Ability to perform numerical simulations and analyze large datasets