ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

Ammin/DET - Scalable Hardware Platforms for the Readout and Control of Qubits

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Supervisor	RIENTE FABRIZIO - fabrizio.riente@polito.it
Contact	GRAZIANO MARIAGRAZIA - mariagrazia.graziano@polito.it ZAMBONI MAURIZIO - maurizio.zamboni@polito.it TURVANI GIOVANNA - giovanna.turvani@polito.it
Context of the research activity	This PhD project focuses on the design and development of scalable FPGA-based hardware platforms for the readout and control of qubits. The research addresses real-time signal generation and acquisition, low-latency feedback, and system-level integration to support multi-qubit architectures. Emphasis is placed on modularity, synchronization, and efficient data processing to enable high-fidelity qubit operations and scalability toward larger quantum processors.
Objectives	The PhD activity will focus on the development of a scalable control and readout platform for quantum processors, with particular emphasis on FPGA-based architectures and their evolution toward custom microelectronic solutions operating at cryogenic temperatures. The work will address the full signal chain required for the coherent control and high-fidelity readout of qubits, including waveform generation, microwave signal processing, data acquisition, and real-time digital feedback. A central objective of the research is the design of hardware architectures that can be progressively migrated from room-temperature FPGA platforms to cryogenic-compatible microelectronic implementations. This includes the investigation of CMOS technologies suitable for cryogenic operation, the co-design of digital and mixed-signal blocks, and the evaluation of performance trade-offs related to power consumption, noise, latency, and reliability at low temperatures. Particular attention will be given to clock distribution, synchronization, and deterministic timing, which are critical for multi-qubit operation and closed-loop quantum control. The platform will be conceived as modular and scalable, enabling the control of increasing numbers of qubits while minimizing wiring complexity and thermal load between temperature stages. The activity will also explore hardware and firmware strategies for implementing qubit-specific control protocols, adaptive measurements, and real-time processing required for

	calibration and error mitigation. An important aspect of the project is the development of a technology-agnostic control architecture capable of interfacing with both superconducting and semiconductor qubit platforms. This will involve the definition of flexible signal generation and readout schemes, as well as abstraction layers that allow the same control infrastructure to be adapted to different qubit modalities. The outcome of the research is expected to contribute to the realization of integrated, cryogenic-aware control systems that support scalable quantum computing architectures.

Skills and competencies for the development of the activity	- Strong background in digital electronics and FPGA-based system design (HDL development, high-speed interfaces, real-time processing) - Knowledge of microelectronic circuit design, with interest in CMOS technologies and operation at cryogenic temperatures - Experience with signal processing for control and readout systems, including mixed-signal and RF concepts - Familiarity with superconducting and/or semiconductor quantum devices and their control requirements - Ability to work at the interface between hardware, firmware, and experimental physics in a multidisciplinary research environment