ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

INFN - Design and testing of integrated electronics for high-resolution timing applications using mixed-signal and digital signal processing-based techniques

Funded By	ISTITUTO NAZIONALE DI FISICA NUCLEARE [P.iva/CF:04430461006]
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Context of the research activity	High-resolution timing systems are essential tools in high-energy physics for time-of-flight particle identification and are increasingly used in industrial and medical applications. In this research project, the candidate will contribute to the design of innovative integrated circuits with high-precision timing capabilities, targeting experiments such as ALICE3 at CERN, DUNE at Fermilab, and INFN R&D initiatives. Both mixed-signal and fully digital approaches will be explored and implemented on silicon.
Objectives	High-resolution timing measurements are becoming pervasive across a wide range of fields, from LIDAR systems for 3D imaging and time-of-flight detection in nuclear medicine to spectrometry in material science. In high-energy physics, these systems are crucial for directly measuring the velocity of relativistic particles, enabling accurate identification of new particles produced in collisions. The candidate will be involved in the design of integrated circuits using deep-submicron technologies with a mixed-signal approach. This includes the development of low-jitter amplifiers, discriminators, and time-to-digital converters (TDCs). A key objective will be the design and characterization of a high-performance timing system for the time-of-flight detector of ALICE 3, a next-generation experiment at the LHC (CERN). The candidate will contribute to the development of a monolithic sensor that integrates, on the same silicon die, the radiation-sensitive area, low-jitter front-end electronics, and high-performance TDCs. The candidate will be introduced to different aspects including radiation-tolerant design, system-level integration, and data management. The candidate will participate in the characterization of sensors and ASICs at INFN facilities as well. For the DUNE experiment at Fermilab, the DENEB 1024-channel integrated circuit currently under development at INFN requires sub-nanosecond timing resolution and outstanding channel modularity. The candidate will help optimize timing-critical circuitry, including trigger logic and clock distribution

	networks, to meet stringent jitter and phase alignment requirements. The expertise developed during these activities is highly valued in the microelectronics industry, particularly in applications requiring high-quality clock signals, such as high-speed ADCs and multi-gigabit transceivers. After gaining experience with various mixed-signal architectures, the candidate will also explore fully digital time pick-off algorithms suitable for implementation on FPGAs and in deep-submicron ASIC technologies. These activities will support innovative R&D projects at INFN. The candidate will be introduced to digital design methodologies using hardware description languages (e.g. VHDL, Verilog) for implementing digital signal processing (DSP) blocks for timing applications. Finally, the candidate will focus on chip-level integration using a digital-on-top flow, addressing the stringent timing and clocking constraints inherent in such systems. Throughout the project, the candidate will use state-of-the-art CAD tools from industry leaders such as Cadence and Synopsys and will be trained in both analog and digital design and verification flows.

Skills and competencies for the development of the activity	A good background in electronics is recommended. Prior experience with timing systems or analog, digital, and mixed-signal ASIC design is not required and will be acquired during the research. Familiarity with hardware description languages (e.g., VHDL, Verilog) is appreciated but not essential. Knowledge of general-purpose programming languages such as Python or C++, along with basic data analysis skills, is encouraged.