ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

CRT/DET - CMOS Integrated Circuits for Digital-Based Sensor Interfaces in Next-Generation Microscale Biosensors

Funded By	DET - Progetti - Progetti ricerca Unione Europea ed Internazionali DET - Progetti - Progetti ricerca MIUR ed altri ministeri FONDAZIONE CRT CASSA DI RISPARMIO DI TORINO [P.iva/CF:06655250014]
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Context of the research activity	The development of biosensors with dimensions comparable to a blood cell, suitable to be internalized in the body to acquire information of clinical interest would have ground-breaking applications in cancer tracking, diagnosis and cure of brain disorders, real-time monitoring of metabolites, biomarkers, drugs and pathogens, and is emerging as the new frontier of biomedical electronics. Turning this vision into reality demands tens-of-micrometers-scale, sub-microwatt power, remotely powered and controlled biosensing chips that are well beyond the state of the art, whose design challenges will be tackled in the framework of this PhD programme taking advantage of new digital-based sensor readout concepts.
	The PhD programme will extensively explore and develop digital-based sensor interfaces and data acquisition techniques as key enablers to overcome the limitations of traditional analog and mixed-signal integrated circuits, so as to meet the requirements of sensor interfaces in microscale biosensing applications, in the framework of the MicroBioNIC PRIN project, and also of neural imaging, in the framework of the EU-funded CEREBRO project. First, the candidate will review previously proposed digital-based analog/mixed signal (AMS) circuit implementations and will be focused on the study of their limitations and on the possibility to overcome them. This objective will be mainly accomplished by refining digital processing algorithms and architectures and/or by post-processing with no additional overhead in terms of silicon area and power. Second, the candidate will study, develop and simulate at schematic level in

Objectives	the Cadence environment new solutions aimed to further reduce the area and power of previous digital-based AMS circuits, to meet the requirements of microscale biosensing and neural signal acquisition. In detail, the partitioning of real-time processing and post-processing tasks will be carefully considered, passives will be suppressed as much as possible, circuit topolgies and control logic will be optimized adopting specific standard cell libraries and taking advantage of digital low power IC design techniques. The performance and the power consumption of the new cells will be extensively simulated, also under process, supply voltage and temperature variations. The solutions developed in the framework of the PhD activity will be finally integrated in a testchip both as standalone cells and in the framework of a complete biosensing platform to monitor specific quantities (e.g. temperature, pH, concentration of metabolites, drugs, biomarkers,..), suitable to be remotely powered and controlled, which will be sent for fabrication. The development of such a platform will involve a strongly multidisciplinary activity in close cooperation with other researchers from other Universities in Italy and abroad taking part in the research projects (in particular at EPFL (CH)), who will develop sensors, energy harvesters and communication modules. The cooperation will involve regular meetings and secondment periods abroad. The single CMOS cells will be validated in the lab by the candidate, who will also actively take part with other researchers in the characterization of the full demonstrator. The results generated by the research activity at each stage will be initially presented in top international conferences in the Solid-State Circuits and Circuits and Systems area, and will be finally published in top journals.

Skills and competencies for the development of the activity	The ideal candidate should have a solid background in CMOS Analog/Mixed-Signal IC Design and should be familiar with the analog and digital IC design flow in the Cadence environment. Previous tapeout experience will be highly appreciated.