

ARTIFICIAL INTELLIGENCE

DAUIN / Integrating Silicon Photonics with Neuromorphic Computing for Enhanced Low-Power AI-Based Edge-Computing Systems

Funded By	Dipartimento di Automatica e Informatica [P.iva/CF:00518460019]
Supervisor	SAVINO ALESSANDRO - alessandro.savino@polito.it
Contact	SAVINO ALESSANDRO - alessandro.savino@polito.it
Context of the research activity	The growing need to transfer massive amounts of data among multitudes of interconnected devices has led to a quest towards low-power and secure approaches to local processing data. Neuromorphic computing, a brain-inspired approach, addresses this need by radically changing information processing. The Ph.D. aims to develop models for the digital twins of neuromorphic neural network accelerators to support the design of next-generation low-power AI-based edge-computing systems coupled with RISC-V-compliant interfaces for smooth adoption and programmability.
	The exponential increase in data transfer demands among interconnected devices necessitates innovative solutions for efficient, low-power, and secure local data processing. Neuromorphic computing, inspired by the brain's information processing methods, offers a transformative approach to meet these demands. This Ph.D. research aims to develop advanced models for digital twins of neuromorphic neural network accelerators, integrating silicon photonics technology to further enhance performance and efficiency.
	Objectives: Develop Digital Twin Models: Create precise digital twin models of neuromorphic neural network accelerators. Ensure these models accurately represent the physical counterparts' behavior and performance. Integrate Silicon Photonics: Incorporate silicon photonics technology into neuromorphic computing systems. Leverage the high-speed, low-power advantages of silicon photonics for data transfer within and between neuromorphic accelerators. Couple with RISC-V Interfaces: Design and implement RISC-V-compliant interfaces for seamless integration and programmability. Ensure compatibility with existing RISC-V architectures to facilitate smooth adoption in various applications.

Optimize for Low-Power Edge-Computing: Focus on developing solutions that significantly reduce power consumption. Target applications in edge-computing environments, where energy efficiency is critical.

Enhance Security and Data Integrity: Incorporate AI-based methods to detect

Objectives	and mitigate potential security vulnerabilities in hardware. Use the flexible and open nature of RISC-V architecture to enhance system security. Methodology: Modeling and Simulation: Utilize advanced simulation tools to develop and validate digital twin models of neuromorphic accelerators integrated with silicon photonics components. Prototyping: Build prototype systems to test the integration of silicon photonics with neuromorphic computing and RISC-V interfaces. Performance Evaluation: Conduct comprehensive performance evaluations, focusing on power efficiency, data transfer speeds, and security aspects. Iterative Design: Use feedback from performance evaluations to iteratively refine the models and prototypes, optimizing for low-power, high-efficiency operation in edge-computing environments. Expected Outcomes: Innovative Models: Creation of robust digital twin models for neuromorphic neural network accelerators incorporating silicon photonics. Enhanced Efficiency: Development of next-generation AI-based edge- computing systems with significantly improved power efficiency and data
	Enhanced Efficiency: Development of next-generation AI-based edge-
	This research will contribute to the advancement of low-power, high- performance AI-based edge-computing systems, leveraging the combined strengths of neuromorphic computing, silicon photonics, and RISC-V architecture.
Skills and	

Skills and	The candidate should have a mix of knowledge of modern computer
competencies	architectures and low-level technologies (in particular silicon photonics) and
for the development of the activity	master programming languages, including C/C++, and Python. An understanding of RISC-V architectures is required.