ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

DET - Analog and Mixed-Signal Integrated Circuits for Non-Conventional Energy-Efficient Machine Learning Accelerators

Funded By	Dipartimento DET
Supervisor	CROVETTI PAOLO STEFANO - paolo.crovetti@polito.it
Contact	MUSOLINO FRANCESCO - francesco.musolino@polito.it CROVETTI PAOLO STEFANO - paolo.crovetti@polito.it
Context of the research activity	The Ph.D. addresses the design of CMOS analog and mixed-signal ICs targeting non-conventional machine learning accelerators. More specifically, a relevant part of the Ph.D. activities will be in the framework of the EU-funded NEUROPULS (Neuromorphic energy-efficient secure accelerators based on phase change materials augmented silicon photonics) project and entail the development of CMOS interfaces from/towards the proof-of-concept photonic accelerator to be developed in the project.
Objectives	The growing need to transfer massive amounts of data among multitudes of interconnected devices for e.g., self-driving vehicles, IoT or industry 4.0 has led to a quest towards low-power and secure approaches to locally processing data. Neuromorphic computing, a brain-inspired approach, addresses this need by radically changing the processing of information. In this context, the EU-funded NEUROPULS project, which involves 14 leading academic/industrial institutions from 8 different countries, aims to build next-generation low-power and secure edge-computing systems by developing novel photonic computing architectures and security layers based on photonic PUFs in augmented silicon photonics CMOS-compatible platforms. The accomplishment of the ambitious goals of the NEUROPULS project entails the development of advanced analog and mixed-signal custom integrated circuits (ICs) in cutting-edge CMOS technologies operating at a multi-GS/s rate, intended to process data to/from the photonic integrated chip developed in the framework of the project, and to interface it with mainstream digital processing units (e.g., FPGAs with ADC and DAC modules). The performance and the power consumption of these blocks is extremely critical since they directly impact the overal performance and the power consumption of the prototype.

	The Ph.D. candidate will be in charge to follow the CMOS IC design tasks in the framework of the NEUROPULS project. In detail, he/she will follow the complete design, integration and testing process of the CMOS analog and mixed-signal ICs which are needed to support the operation of the photonic accelerator developed in the framework of the project and to allow its interaction with conventional CMOS digital electronic circuits. Starting from the insight gained in the framework of the NEUROPULS project, the Ph.D. candidate will also have the occasion to contribute original researches in the framework of non-convention CMOS machine learning HW accelerators based on innovative analog or mixed-signal architectures.

Skills and competencies for the development of the activity	A strong motivation and an excellent academic background in CMOS IC design are needed. In particular, the candidate should be familiar with the analog/mixed-signal/RF IC design and simulation flow (Cadence environment) and should have tapeout experience in nanoscale CMOS.