ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

MUR DM 117/Ideas&Motion - Logic-In-Memory DataFlow Architectures for high performance low power applications

Funded By	MINISTERO DELL'UNIVERSITA' E DELLA RICERCA [P.iva/CF:97429780584] Ideas & Motion s.r.l. [P.iva/CF:03463330047] Politecnico di TORINO [P.iva/CF:00518460019]
Supervisor	ZAMBONI MAURIZIO - maurizio.zamboni@polito.it
Contact	GRAZIANO MARIAGRAZIA - mariagrazia.graziano@polito.it VACCA MARCO - marco.vacca@polito.it Claudio Genta claudio.genta@ideasandmotion.com
Context of the research activity	Study and design of hardware accelerators that exploits the Logic-In-Memory paradigm to speed-up the execution of DataFlow Algorithms improving the performance and reducing at the same time power consumption Progetto finanziato nell'ambito del PNRR – DM 117/2023 - CUP E14D23002000004
	The development of dedicated hardware accelerators to execute specific algorithms is nowadays becoming a necessity to process in real time the huge amount of data required by demanding applications, for example autonomous driving or biomedical and aerospace applications. Typically these hardware accelerators are used together with general purpose processors in the so called Systems On Chip, to speed up the execution of specific and high demanding algorithms. Given the importance of machine learning it is quite common to find dedicated hardware accelerators for deep neural network inference alongside standard processors. Unfortunately, traditional Von Neumann architectures are not able to provide the required level of performance, since improving the speed normally also implies an increment of power consumption, which is not compatible with the requirement of many battery powered devices and it is in contrast with the green transition that our world is undergoing. DataFlow architectures may represent a good alternative to Von Neumann architectures to create energy efficient and fast hardware accelerators. They

Objectives	are particularly suited to implement neural networks and more in general machine learning algorithms. To further improve the efficiency of the systems, DataFlow architectures can be coupled with the Logic-In-Memory principle, where logic and memory elements are combined together to solve the communication bottleneck between logic processors and memories. Combining these two principles it is possible to create partially configurable hardware accelerators that can speed up the execution of the algorithms. However, the complexity of these systems and the use of highly scaled electronic devices, makes the use of verification and optimization techniques mandatory. The goal of this PhD project is therefore: To study and develop new DataFlow architectures based on the Logic-In-Memory principle, to minimize power consumption due to the data movement between logic and memory, improving at the same time the algorithm execution time. The goal is to develop hardware accelerators to be integrated inside microcontrollers to be used in automotive applications, particularly adapted to accelerate machine learning algorithms. -To develop and use advanced functional verification systems to test the circuits reducing the risks of malfunctioning or unwanted circuit behaviors. -To define a methodology to design and study Logic-In-Memory architectures to understand which is the better approach to follow for each application and algorithm, without the need of fully designing the circuits, greatly reducing the development times for new architectures. -To apply the developed methodology and architectures to safety-critical applications, for example autonomous driving.

Skills and competencies for the development of the activity	-VHDL language; -Digital architectures design; -Basic programming language knowledge; -Experience in the development of hardware accelerators for neural networks is welcome; -FPGA knowledge and programming experience.