COMPUTER AND CONTROL ENGINEERING

MUR DM 117/Synopsys - Methodologies for next generation FuSa/Soft Errors analysis and verification

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Context of the research activity	Functional Safety (FuSa) is a concept applied in safety-critical domains for years. As new hardware and software paradigms are emerging (e.g., due to ADAS or high-performance applications for space), current FuSa workflows will soon become obsolete. This research aims to develop innovative FuSa methodologies by introducing new solutions for analyzing Soft Errors and their impact on safety, new safety mechanisms, and automatic verification methods to integrate into next-generation EDA tools. Progetto finanziato nell'ambito del PNRR - DM 117/2023 -CUP E14D23002020004
	New hardware and software paradigms and emerging technologies will pose severe challenges to the current Functional Safety (FuSa) workflows. Some examples: - In cyber-physical systems and IoT devices, it can be challenging to ensure the safety in the presence of cyber-attacks. - Artificial intelligence is being used in safety-critical systems, and can introduce new risks, such as the possibility of unintended consequences. - In Edge computing, ensuring safety in the presence of limited resources and connectivity can be difficult. As these technologies continue to evolve, developing new methods for ensuring the safety of next-generation safety-critical systems is essential. Research objectives The research will focus on advancing state-of-the-art Functional Safety, defining failure modes, safety mechanisms, and evaluation methods, specifically emphasizing emerging hardware and software paradigms.

Objectives	Summarizing, the objectives of the research will be: - Analyzing the current functional safety standards, such as ISO 26262 and IEC 61508, and state-of-the-art EDA tools for FuSa and reliability evaluation, identifying their weaknesses when dealing with the next-generation safety-critical systems. - Developing innovative soft error analysis methodologies based on available and new safety mechanisms and verifying them formally or empirically. - Prototyping an overall qualification flow for safety-critical systems to guide the development of next-generation EDA tools for FuSa insertion and assessment. This research is aligned with the goals of the National Centers on Sustainable Mobility and HPC, as well as the Extended Partnership on Artificial Intelligence, which further emphasizes its significance in advancing the state-of-the-art in this field. Outline of possible research plan First year: The candidate will study the main functional safety standards used in various domains. They will also identify suitable hardware and software to use in their experiments. In this first year, it would be essential to learn about the state-of-the-art on FuSa and dependability in general (including the overlapping with cybersecurity for specific domains). Moreover, the candidate will conduct experiments using commercial EDA tools on the identified platform. Second year: The candidate will develop new techniques to enhance the traditional soft error analysis workflow supported by available EDA tools. As the objective is to face with limitations of those tools, they will expose scalability and technological-related issues. In cooperation with Synopsys, the candidate will work on prototyping innovative methodologies for the insertion of proper safety mechanisms, their verification, and the evaluation of their impact on reliability metrics. Third year: The candidate will automatize the developed methodology and validate the overall qualification flow on industrial test cases, possibly from Synopsys' partners or open source. As the research group is involved in activities with RISC-V communities, such as OpenHW, the candidate will be involved in open-source projects on the safety and security of RISC-V, where they can further test the developed framework. List of possible venues for publications Different venues for publications will be considered, which could include: - IEEE ToC, TVLSI, TCAD - ICCAD, ITC, ETS, DATE, RISC-V Summit, SNUG
Skills and competencies for the development of the activity	- Background in CPU architectures. - Digital Design knowledge, from the RTL to the Physical implementation stage. - Deep knowledge of testing, fault assessment and modeling strategies. - Good knowledge of industrial EDA tools and the ability to rapidly learn new

the activity	ones.