COMPUTER AND CONTROL ENGINEERING

MUR DM 117/STMicroelectronics - Innovative techniques to improve the reliability of embedded and HPC systems

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Context of the research activity	This research focuses on the importance of reliable and fault-tolerant electronic devices in embedded and HPC systems used in various fields such as mobility, medical devices, and infrastructure. To improve the testing techniques for these circuits, the research proposes innovative approaches that cover not only the digital part but also the analog and mixed-signal interconnections. The study addresses the challenges posed by the delay and internal defects in logic gates, and the effects of aging and external factors on device performance. The research utilizes tools and technologies provided by STMicroelectronics to develop field testing algorithms and methodologies. Progetto finanziato nell'ambito del PNRR - DM 117/2023 - CUP E14D23002020004
	Research objectives The massive use of electronic devices in embedded and HPC systems, places great emphasis on the reliability and tolerance to hardware faults that such devices offer. Defect affecting the hardware are increasingly harder to detect due to the complexity of electronic systems and emerging technologies, and this creates serious criticalities on the system's operational life: as faults can manifest themselves as wrong data, they may severely affect the software making use of the faulty hardware. The is the need for improving the effectiveness of the state-of-the-art evaluation methods, as well as test strategies to identify and mitigate those faults. The objectives of this research are summarized in the following. - Develop a fault grading framework for defect-oriented faults models for

Objectives	digital circuits (such as path-delay or cell-aware faults), as dealing with those faults is only partially supported by commercial EDA tools. A fault grading process is of paramount importance for understanding the effectiveness of state-of-the-art test methods. - Assess the effectiveness of state-of-the-art test methods in detecting defect-oriented faults. - Analyze the impact of defect-oriented faults on the final system's reliability, considering microprocessor-based systems as reference, and including the interconnection between analog and digital logic. - Contribute to the development of new algorithms for defect-oriented fault testing of microprocessor-based systems, in the form of on software-based self-test or making use of special design-for-test features. Outline of possible research plan First year: The candidate will begin by conducting a comprehensive literature review of defect-oriented test methods for digital circuits and developing a suitable fault grading framework. They will also review previous work by other PhD students in the research group on modelling cell-aware faults on open and proprietary technology libraries from STMicroelectronics. The candidate will then create a set of test cases to assess the effectiveness of existing state-of-the-art test methods for detecting defect-oriented faults. They will use the new framework to compare and evaluate these test methods. Second year: In the second year, the candidate will focus on designing and implementing new test algorithms to improve the fault coverage of defect-oriented faults on microprocessor-based systems. They will build upon existing software-based self-test techniques developed for less complex fault models and investigate the propagation of errors through interconnections between analog and digital logic. The candidate will also develop proper mitigation methods to improve the system's reliability. They will validate the effectiveness of the new algorithms on a set of benchmarks and compare them with existing state-of-the-art test methods. Third year: In the final year, the candidate will conduct simulations and experiments to analyze the impact of defect-oriented faults on the reliability of microprocessor-based systems. They will also investigate existing design-for-test features and design ad-hoc hardware to further improve the system's reliability. The candidate will conduct experiments on real-world systems provided by STMicroelectronics to validate the effectiveness of the proposed techniques. List of possible venues for publications The candidate will prepare and submit papers to top-tier conferences and journals in the field of electronic systems, embedded systems, and fault tolerance. Possible venues for publications could include: - IEEE Transactions on Computers - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems - IEEE Transactions on Very Large Scale Integration (VLSI) Systems - International Conference on Computer-Aided Design (ICCAD) - International Test Conference (ITC)

	- IEEE European Test Symposium (ETS) - IEEE International Symposium on Circuits and Systems (ISCAS) - Design, Automation and Test in Europe Conference (DATE) Projects The research is consistent with the themes of the National Centers on Sustainable Mobility and HPC, as well as with those of the Extended Partnership on Artificial Intelligence, in which members of the CAD group participate.

Skills and competencies for the development of the activity	- Solid background in digital circuits and microprocessor-based systems design and testing - Experience with fault modeling and testing techniques for digital circuits, such as stuck-at faults, transition faults, and path-delay faults. - Knowledge of EDA tools, particularly for fault simulation.