ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

Full-Stack System-on-Chip Optimization

Funded By	Dipartimento DET
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Context of the research activity	The research carried out by the PhD candidate will be in the area of System-on-Chip modeling, design, and optimization. A holistic approach that starts from the application down to the final chip tape-out will be used in order to address the complexity and challenges associated with advanced electronic systems, with the goal of optimizing performance, power efficiency, reliability, and design productivity. A design approach will be pursued, based on multi-FPGA scalable platforms together with a task-level resource allocation and scheduling algorithm to efficiently and automatically trade-off performance, resources, and energy per operation
	A full-stack approach to System-on-Chip (SoC) design is crucial in addressing the complexity and challenges associated with designing advanced electronic systems. This approach recognizes the interdependencies and interactions between different design layers and components, leading to more efficient and effective solutions. 1) Performance Optimization: By considering the full stack, it is possible to optimize performance at multiple levels. For instance, optimizing the hardware architecture and design can lead to improved throughput and latency. At the same time, software optimizations, such as algorithmic improvements or parallelization techniques, can further enhance the overall system performance. 2) Power Efficiency: A full-stack approach enables power optimization at different levels, including low-level circuit design, architectural choices, and software algorithms. 3) System Reliability: Complex electronic systems face various challenges related to reliability, including noise, thermal effects, and voltage and process variations. By taking a full-stack approach, designers can consider reliability enhancements at each level of the SoC design. This includes error correction mechanisms, fault-tolerant designs, and robust software implementations. 4) Design Productivity: A full-stack approach provides opportunities for abstraction and automation, allowing designers to leverage high-level synthesis, EDA tools, and machine learning techniques. This streamlines the design process, reduces design iterations and the associated costs, and enhances overall productivity.

Objectives	To enable a full-stack approach to SoC design, this PhD research will focus on creating and/or optimizing the various links between the various stages of the design flow. 1) Application designers often ignore the characteristics of the underlying hardware, which leads either to performance or power inefficiency or to degradation of the quality of results. By incorporating hardware abstractions and models in the application tools, the PhD candidate will help avoid this pitfall: as an example, the hardware costs (area, energy) of components can be considered in the selection of a Machine-Learning (ML) algorithm and in its hardware-optimized training way before the actual implementation as an SoC ML accelerator. 2) From the application to the Register-Transfer Level (RTL) design, a fast and reliable Design-Space Exploration (DSE) is needed to determine the best alternatives in terms of cost and performance. The PhD candidate will contribute to extending to ASIC SoCs a DSE framework originally developed in the research team of the supervisor for FPGA SoCs. For example, the DSE will be improved to select the best alternative between actual execution of the application in a dedicated accelerator, or in the CPU of the SoC. 3) To improve the fidelity of the high-level DSE, details of the low-level optimizations must be abstracted and modeled. By experimenting with the low-level flow from RTL to layout with specific benchmarks, the PhD candidate will work on creating area, performance and power models that can be reliably used at the higher design levels. In this context, the candidate will contribute to improving a latch-based low-level implementation technique developed by the research team of the supervisor.

Skills and competencies for the development of the activity	The candidate is required to have skills and competences such as those typically obtained with a Master of Science degree in areas like Electronic Engineering or Computer Engineering. In addition, the candidate should possess a proven experience with the ASIC design flow (RTL, logic synthesis, layout tools).