ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

PNRR - Design of hardware efficient decoders for Ultra-reliable low latency communication

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Context of the research activity	Ultra-reliable low latency communication (URLLC) combines powerful error correcting capability and low decoding latency. The most important known coding schemes (including turbo, LDPC, and polar codes) as well as their decoding algorithms need to be revisited from a new perspective, which assumes the latency as one of the key specifications. In this scenario, new hardware efficient decoding architectures must be investigated to achieve the desired limits of latency, reliability, and power dissipation. Progetto finanziato nell'ambito del PNRR - PE14 - RESTART, Spoke 3 (POLIMI): Structural 6G (Tema6) - CUP: E13C22001870001
	Ultra-Reliable Low Latency Communications (URLLC) was introduced in the context of the 5G networks, particularly for mission-critical applications, which require a guaranteed connection and low latency, such as for example self-driving cars and remote surgery. Smart factories and Industry 4.0 have similar requirements, where machinery and robotics need to interact with each other in real time. They might also require real-time information from other sensors across the manufacturing facility. Low-latency systems allow these machine-operated systems to work safely and efficiently to enhance production lines. In these applications, the network reliability can be higher than 99.999% and the transmission latency can be lower than 1 ms. URLLC may also be of interest for high-reliability applications on the Internet of Things (IoT), where the low energy implementation is an additional severe constraint. To ensures these objectives, several novel features are required, including efficient data transfer protocols, and shorter transmissions on larger subcarriers. The Forward Error Correction (FEC) system is one of the most important and most critical elements is a reliable communication system. It is responsible for

Objectives	a large percentage of the overall communication latency; moreover, channel decoders working with modern error correction codes are complex and power-hungry components. Basically, all FEC systems studied and implemented in the past were conceived by adopting design methodologies aimed at optimizing the throughput, rather than the latency. Therefore, there is the need of developing a completely new approach to the design of FEC systems targeting the latency objective, together with reliability and efficiency (especially from the power dissipation point of view). The planned PhD activity will focus on the exploration of novel decoding architectures specifically oriented to the latency minimization, and it will be strictly coordinated with a separate doctorate activity, which will investigate on new low-latency error-correcting codes and their decoding algorithms. Thus, the two doctorate students will jointly study and optimize a FEC system and its hardware implementation, with the objective to propose a novel URLLC solution surpassing the known approaches in terms of error correction capability, latency, and hardware efficiency. The outcomes of the activity will be a high-level simulative model and an accurate hardware model synthesizable on an FPGA platform. The ASIC implementation will also be completed at least till the layout level, to fully characterize a dedicated Silicon component in terms of occupied area, delay, and power dissipation. Progetto finanziato nell'ambito del PNRR, Codice Unico di Progetto (CUP) E13C22001870001

Skills and competencies for the development of the activity	Design of digital hardware. Architectures for digital signal processing. Knowledge of hardware description languages and design tools.