ELECTRICAL, ELECTRONICS AND COMMUNICATIONS ENGINEERING

Active gate drivers for last generation GaN HEMTs

Funded By	Dipartimento DET
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Context of the research activity	The research deals with the smart driving of last generation high voltage GaN HEMTs aimed to address power efficiency, electromagnetic compatibility and reliability issues in HV power modules.
Objectives	Switching legs based on last generation HV GaN power transistors are able to switch HV DC input (e.g., 600V) in less than 3ns, which is much shorter than that obtained with previous technologies. This means that, power circuits based on such devices can switch faster thus getting higher power density and comparable power loss. However, such improvements can be achieved by driving the power device properly. Indeed, traditional isolated gate drivers like those used to drive MOS or SiC transistors, do not provide the expected performance. The research activity consists in a in-depth characterization of e-mode GaN HEMTs that will provide the information needed to design of a smart gate driver capable of getting the most out in terms of power efficiency while mitigating the switching noise. The circuit will be also able to manage under/over voltages as well as to address self immunity issues. A test chip will be design referring to a last generation HV CMOS technology, then it will be fabricated and experimentally characterized.
Skills and competencies for the development of the activity	The successful candidate should have good knowledge of circuit theory, CMOS technology, analysis and design of analog and digital integrated circuits, signal and power integrity. The knowledge of design tools such as Cadence Virtuoso is a plus.